Fast ±150mA Power Buffer

FEATURES

- 20MHz Bandwidth
- 75V/μs Slew Rate
- Drives ±10V into 75Ω
- 5mA Quiescent Current
- Drives Capacitive Loads >1μF
- Current and Thermal Limit
- Operates from Single Supply ≥4.5V
- Very Low Distortion Operation

APPLICATIONS

- Boost Op Amp Output
- Isolate Capacitive Loads
- Drive Long Cables
- Audio Amplifiers
- Video Amplifiers
- Power Small Motors
- Operational Power Supply
- FET Driver

DESCRIPTION

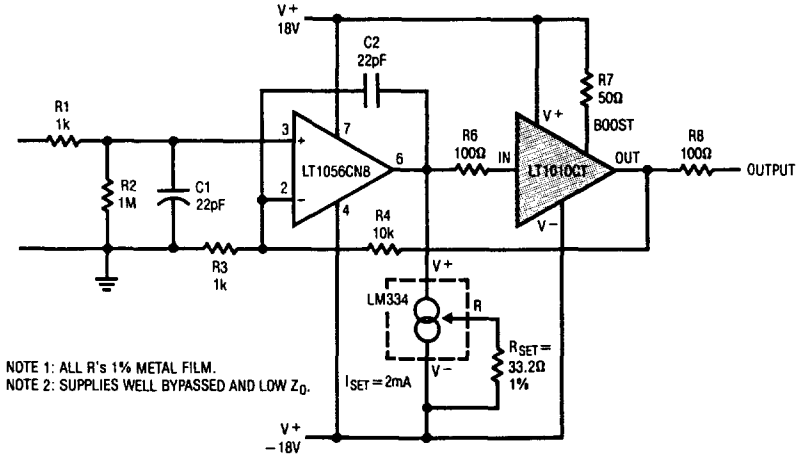
The LT1010 is a fast, unity-gain buffer that can increase the output capability of existing IC op amps by more than an order of magnitude. This easy-to-use part makes fast amplifiers less sensitive to capacitive loading, reduces thermal feedback in precision dc amplifiers and is recommended for a wide range of fast and slow applications.

Designed to be incorporated within the feedback loop, the buffer can isolate almost any reactive load. Internal operating currents are essentially unaffected by supply or output voltage, accounting for the 4.5V to 40V supply voltage range with unchanged specifications. Single-supply operation is also practical.

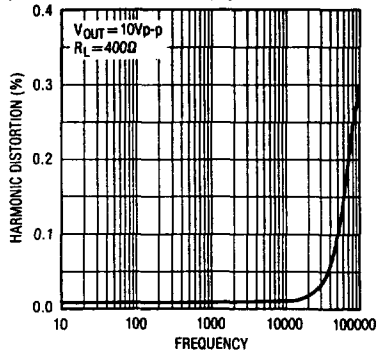
This monolithic IC is supplied in an 8-pin miniDIP and three standard power packages: the solid kovar base TO-5 (TO-39), the steel TO-3 and the plastic TO-220. The low thermal resistance power packages are an aid in reducing operating junction temperatures. With the TO-3, TO-220, and miniDIP packages, an option is available to raise quiescent current and improve speed. The miniDIP version is supplied for those applications not requiring high power dissipation or where board space is a premium.

In the TO-39 package, the LT1010 can sometimes replace the hybrid LH0002. With the exception of speed it exceeds key specifications and fault protection is vastly superior. Further, the lower thermal resistance package and higher maximum operating temperature of the new monolithic circuit allow more usable output.

Very Low Distortion Buffered Pre-Amplifier



NOTE 1: ALL R's 1% METAL FILM.
NOTE 2: SUPPLIES WELL BYPASSED AND LOW Z_O.



ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage ..... ±22V
Continuous Output Current ..... ±150mA
Continuous Power Dissipation (Note 1)
- LT1010MK 5.0W
- LT1010CK 4.0W
- LT1010CT 4.0W
- LT1010MH 3.1W
- LT1010CH 2.5W
- LT1010CN8 ..... 0.75W

Input Current (Note 2) ..... ±40mA
Operating Junction Temperature
- LT1010M ..... –55°C to 150°C
- LT1010C ..... 0°C to 125°C

Storage Temperature ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec.) ..... 300°C

PRECONDITIONING

100% Thermal Limit Burn in

PACKAGE/ORDER INFORMATION

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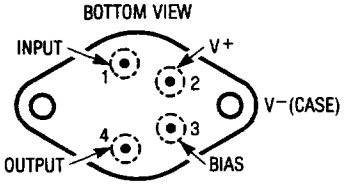
<td> 

K PACKAGE
4-LEAD TO-3 METAL CAN
(STEEL)</td>
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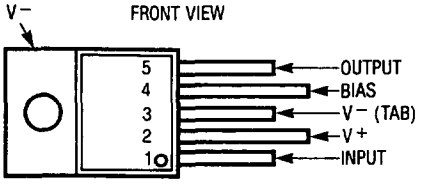
LT1010MK
LT1010CK</td>
<td> 

T PACKAGE
5-LEAD TO-220 PLASTIC</td>
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LT1010CT</td>
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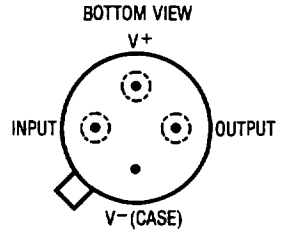
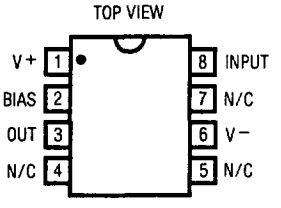
<td> 

H PACKAGE
4-LEAD TO-39 METAL CAN
(KOVAR BASE)</td>
<td>LT1010MH
LT1010CH</td>
<td> 

N PACKAGE
8-LEAD PLASTIC DIP</td>
<td>LT1010CN8</td>
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ELECTRICAL CHARACTERISTICS (See Note 3. Typical values in curves)

SYMBOL	PARAMETER	CONDITIONS (NOTE 3)		LT1010M MIN	LT1010M MAX	LT1010C MIN	LT1010C MAX	UNITS
V_{OS}	Output Offset Voltage	Note 3		20	110	0	150	mV
			●	−10	220	−20	220	mV
		$V_S = \pm 15V$, $V_{IN} = 0$		40	90	20	100	mV
I_B	Input Bias Current	$I_{OUT} = 0$		0	150	0	250	µA
		$I_{OUT} \leq 150mA$		0	250	0	500	µA
			●	0	300	0	800	µA
A_V	Large Signal Voltage Gain		●	0.995	1.00	0.995	1.00	V/V
R_{OUT}	Output Resistance	$I_{OUT} = \pm 1mA$		6	9	5	10	Ω
		$I_{OUT} = \pm 150mA$		6	9	5	10	Ω
			●		12		12	Ω
	Slew Rate	$V_S = \pm 15V$, $V_{IN} = \pm 10V$						
		$V_{OUT} = \pm 8V$, $R_L = 100\Omega$		75		75		V/µs
V_{SOS}^+	Positive Saturation Offset	Note 4, $I_{OUT} = 0$			1.0		1.0	V
			●		1.1		1.1	V
V_{SOS}^-	Negative Saturation Offset	Note 4, $I_{OUT} = 0$			0.2		0.2	V
			●		0.3		0.3	V
R_{SAT}	Saturation Resistance	Note 4, $I_{OUT} = \pm 150mA$			18		22	Ω
			●		24		28	Ω
V_{BIAS}	Bias Terminal Voltage	Note 5, $R_{BIAS} = 20\Omega$		750	810	700	840	mV
			●	560	925	560	880	mV
I_S	Supply Current	$I_{OUT} = 0$, $I_{BIAS} = 0$			8		9	mA
			●		9		10	mA

Note 1: For case temperatures above 25°C, dissipation must be derated based on a thermal resistance of 25°C/W with the K and T packages, 40°C/W with the H package, and 130°C/W for N8 package for *ambient* temperatures above 25°C. See applications information.

Note 2: In current limit or thermal limit, input current increases sharply with input-output differentials greater than 8V; so input current must be limited. Input current also rises rapidly for input voltages 8V above V^+ or 0.5V below V^-.

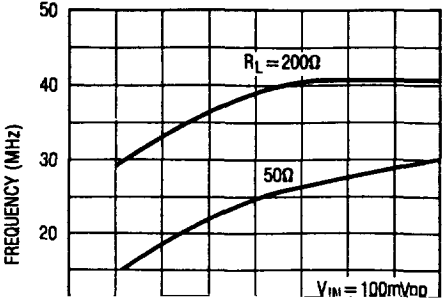
Note 3: Specifications apply for $4.5V \leq V_S \leq 40V$, $V^- + 0.5V \leq V_{IN} \leq V^+ - 1.5V$ and $I_{OUT} = 0$, unless otherwise stated. Temperature range is $-55°C \leq T_j \leq 150°C$, $T_C \leq 125°C$, for the LT1010M and $0°C \leq T_j \leq 125°C$, $T_C \leq 100°C$, for the LT1010C. The ● denotes the specifications that apply over the full temperature range.

Note 4: The output saturation characteristics are measured with 100mV output clipping. See applications information for determining available output swing and input drive requirements for a given load.

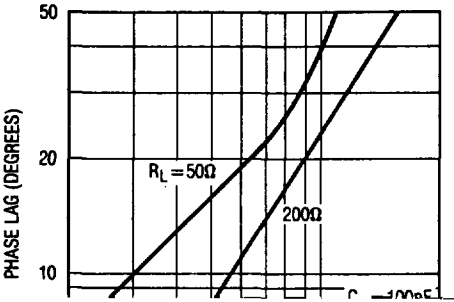
Note 5: With the TO-3 and TO-220 packages, output stage quiescent current can be increased by connecting a resistor between the bias pin and V^+. The increase is equal to the bias terminal voltage divided by this resistance.

TYPICAL PERFORMANCE CHARACTERISTICS

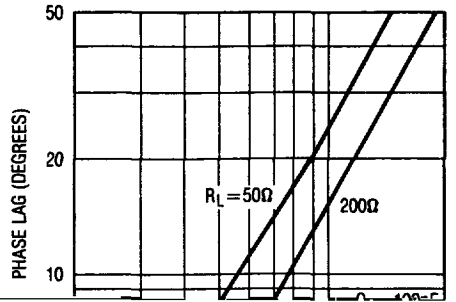
Bandwidth



Phase Lag

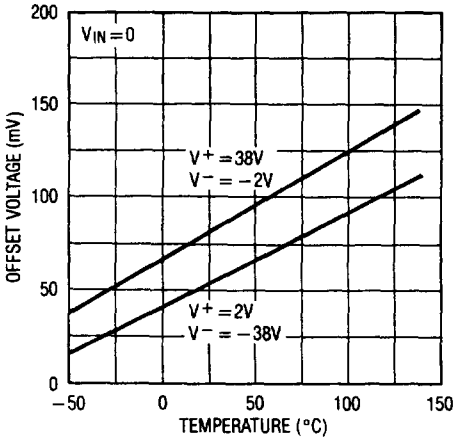


Phase Lag

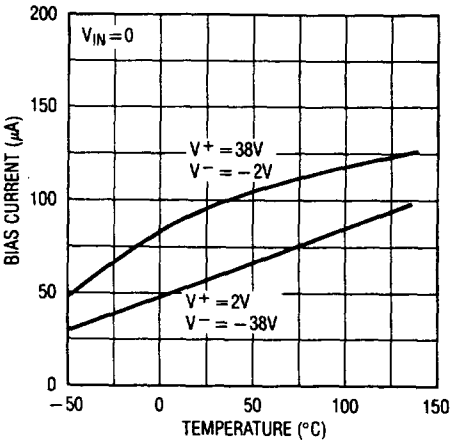


TYPICAL PERFORMANCE CHARACTERISTICS

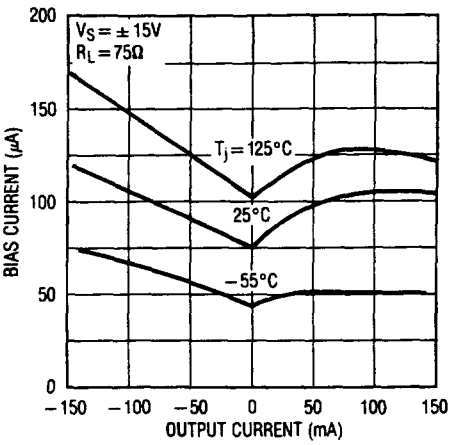
Output Offset Voltage



Input Bias Current



Input Bias Current



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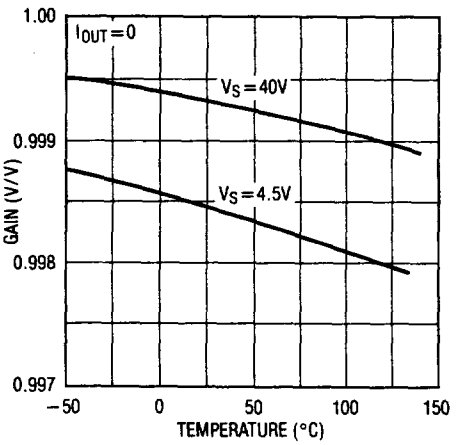
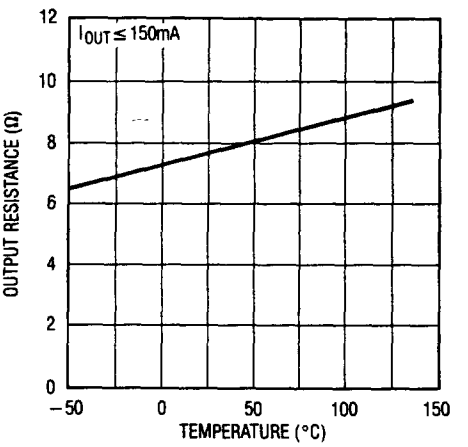
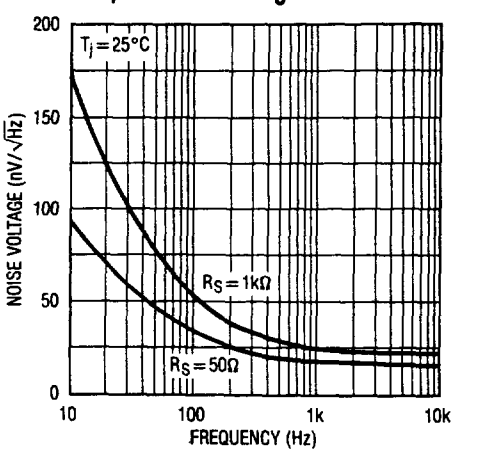
Voltage Gain



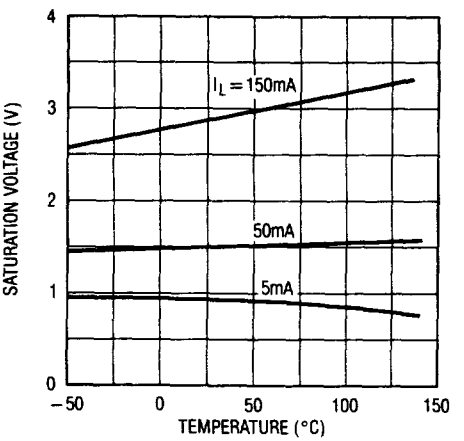
Output Resistance



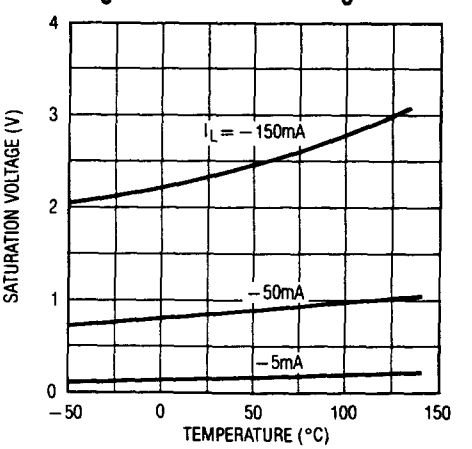
Output Noise Voltage



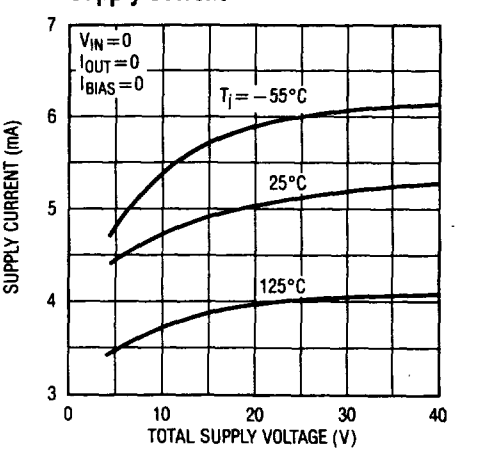
Positive Saturation Voltage



Negative Saturation Voltage

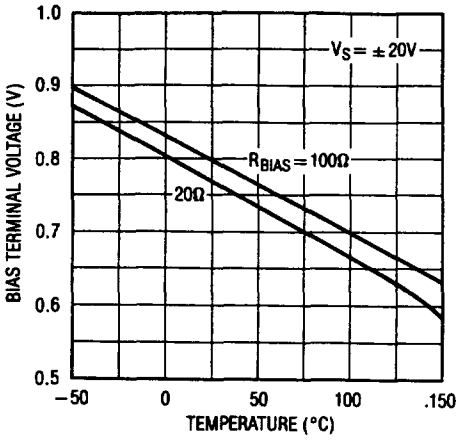


Supply Current

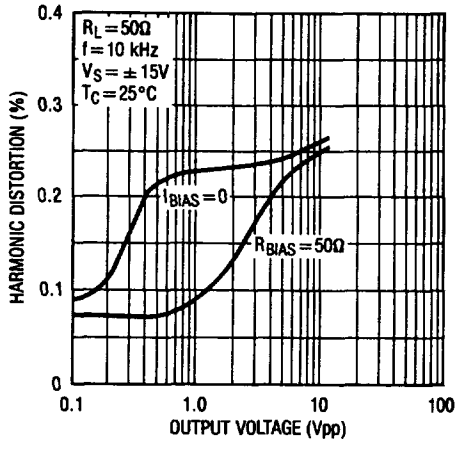


TYPICAL PERFORMANCE CHARACTERISTICS

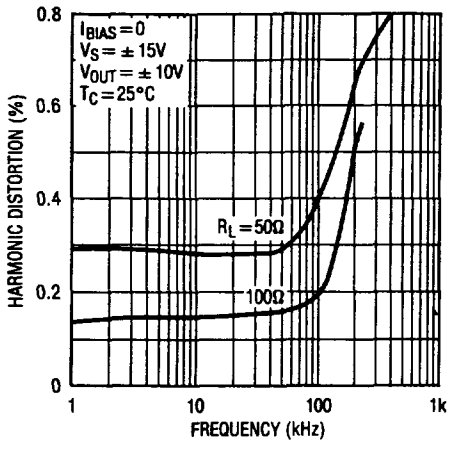
Bias Terminal Voltage



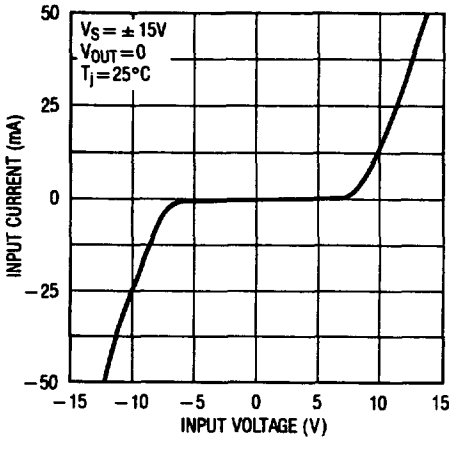
Total Harmonic Distortion



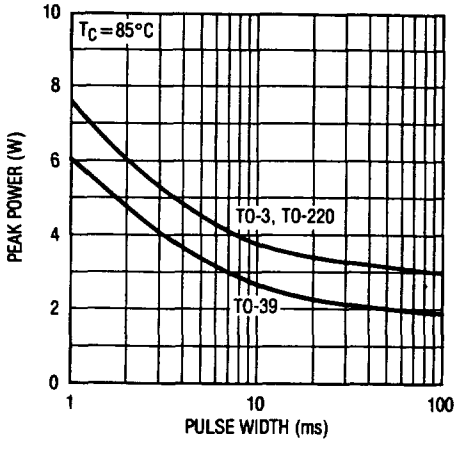
Total Harmonic Distortion



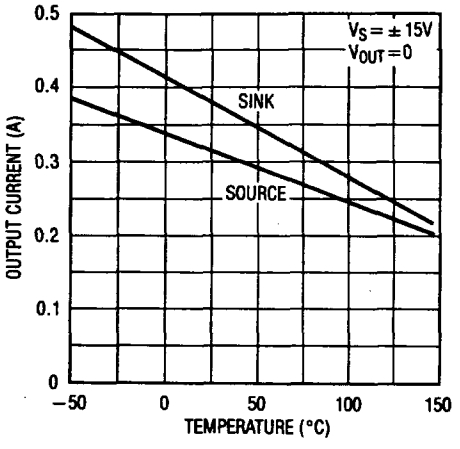
Shorted Input Characteristics



Peak Power Capability



Peak Output Current



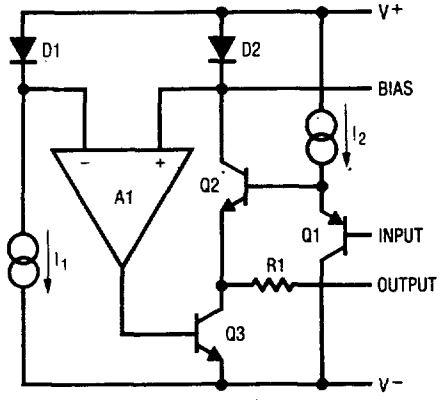
APPLICATIONS INFORMATION

General

These notes briefly describe the LT1010 and how it is used; a detailed explanation is given elsewhere*. Emphasis here will be on practical suggestions that have resulted from working extensively with the part over a wide range of conditions. A number of applications are also outlined that demonstrate the usefulness of the buffer beyond that of driving a heavy load.

Design Concept

The schematic below describes the basic elements of the buffer design. The op amp drives the output sink transistor, Q3, such that the collector current of the output follower, Q2, never drops below the quiescent value (determined by I_1 and the area ratio of D1 and D2). As a result, the high frequency response is essentially that of a simple follower even when Q3 is supplying the load current. The internal feedback loop is isolated from the effects of capacitive loading by a small resistor in the output lead.

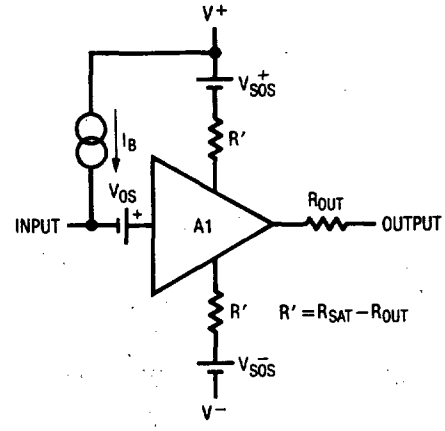


The scheme is not perfect in that the rate of rise of sink current is noticeably less than for source current. This can be mitigated by connecting a resistor between the bias terminal and V^+, raising quiescent current. A feature of the final design is that the output resistance is largely independent of the follower quiescent current or the output load current. The output will also swing to the negative rail, which is particularly useful with single-supply operation.

*R. J. Widlar, "Unique IC Buffer Enhances Op Amp Designs; Tames Fast Amplifiers," *Linear Technology Corp. TP-1*, April, 1984.

Equivalent Circuit

Below 1MHz, the LT1010 is quite accurately represented by the equivalent circuit shown here for both small and large signal operation. The internal element, A1, is an idealized buffer with the unloaded gain specified for the LT1010. Otherwise, it has zero offset voltage, bias current and output resistance. Its output also saturates to the internal supply terminals†.



Loaded voltage gain can be determined from the unloaded gain, A_V, the output resistance, R_{OUT}, and the load resistance, R_L, using:

$$A_{VL} = \frac{A_V R_L}{R_{OUT} + R_L}$$

Maximum positive output swing is given by:

$$V_{OUT}^+ = \frac{(V^+ - V_{SOS}^+) R_L}{R_{SAT} + R_L}$$

The input swing required for this output is:

$$V_{IN}^+ = V_{OUT}^+ \left(1 + \frac{R_{OUT}}{R_L}\right) - V_{OS} + \Delta V_{OS},$$

where ΔV_{OS} is the 100mV clipping specified for the saturation measurements. Negative output swing and input drive requirements are similarly determined.

† See electrical characteristics section for guaranteed limits.

APPLICATIONS INFORMATION

Supply Bypass

The buffer is no more sensitive to supply bypassing than slower op amps, as far as stability is concerned. The 0.1μF disc ceramic capacitors usually recommended for op amps are certainly adequate for low frequency work. As always, keeping the capacitor leads short and using a ground plane is prudent, especially when operating at high frequencies.

The buffer slew rate can be reduced by inadequate supply bypass. With output current changes much above 100mA/μs, using 10μF solid tantalum capacitors on both supplies is good practice, although bypassing from the positive to the negative supply may suffice.

When used in conjunction with an op amp and heavily loaded (resistive or capacitive), the buffer can couple into supply leads common to the op amp causing stability problems with the overall loop and extended settling time. Adequate bypassing can usually be provided by 10μF solid tantalum capacitors. Alternately, smaller capacitors could be used with decoupling resistors. Sometimes the op amp has much better high frequency rejection on one supply, so bypass requirements are less on this supply.

Power Dissipation

In many applications, the LT1010 will require heat sinking. Thermal resistance, junction to still air is 150°C/W for the TO-39 package, 100°C/W for the TO-220 package, 60°C/W for the TO-3 package, and 130°C/W for the miniDIP package. Circulating air, a heat sink, or mounting the package to a printed circuit board will reduce thermal resistance.

In dc circuits, buffer dissipation is easily computed. In ac circuits, signal waveshape and the nature of the load determine dissipation. Peak dissipation can be several times average with reactive loads. It is particularly important to determine dissipation when driving large load capacitance.

With ac loading, power is divided between the two output transistors. This reduces the effective thermal resistance, junction to case, to 30°C/W for the TO-39 package and 15°C/W for the TO-3 and TO-220 packages, as long as the peak rating of neither output transistor is exceeded. The typical curves indicate the peak dissipation capabilities of one output transistor.

Overload Protection

The LT1010 has both instantaneous current limit and thermal overload protection. Foldback current limiting has not been used, enabling the buffer to drive complex loads without limiting. Because of this, it is capable of power dissipation in excess of its continuous ratings.

Normally, thermal overload protection will limit dissipation and prevent damage. However, with more than 30V across the conducting output transistor, thermal limiting is not quick enough to insure protection in current limit. The thermal protection is effective with 40V across the conducting output transistor as long as the load current is otherwise limited to 150mA.

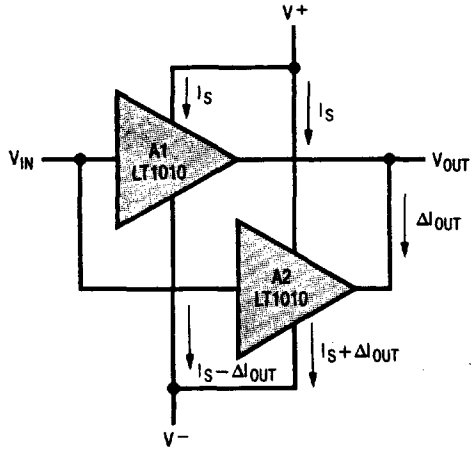
Drive Impedance

When driving capacitive loads, the LT1010 likes to be driven from a low source impedance at high frequencies. Certain low power op amps (e.g., the LM10) are marginal in this respect. Some care may be required to avoid oscillations, especially at low temperatures.

Bypassing the buffer input with more than 200pF will solve the problem. Raising the operating current also works, but this cannot be done with the TO-39 package.

APPLICATIONS INFORMATION

Parallel Operation



Parallel operation provides reduced output impedance, more drive capability and increased frequency response under load. Any number of buffers can be directly paralleled as long as the increased dissipation in individual units caused by mismatches of output resistance and offset voltage is taken into account.

When the inputs and outputs of two buffers are connected together, a current, ΔI_{OUT}, flows between the outputs:

$$\Delta I_{OUT} = \frac{V_{OS1} - V_{OS2}}{R_{OUT1} + R_{OUT2}},$$

where V_{OS} and R_{OUT} are the offset voltage and output resistance of the respective buffers.

Normally, the negative supply current of one unit will increase and the other decrease, with the positive supply current staying the same. The worst case $(V_{IN} - V^+)$ increase in standby dissipation can be assumed to be $\Delta I_{OUT}\, V_T$, where V_T is the total supply voltage.

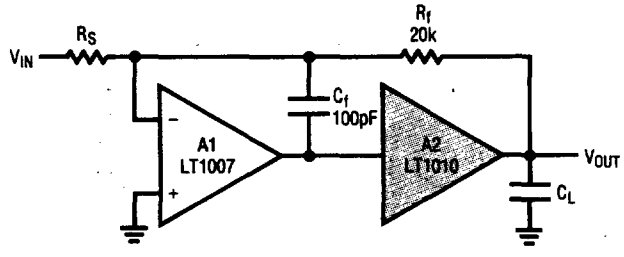
Offset voltage is specified worst case over a range of supply voltages, input voltage and temperature. It would be unrealistic to use these worst case numbers above because paralleled units are operating under identical conditions. The offset voltage specified for $V_S = \pm 15V$, $V_{IN} = 0$ and $T_A = 25°C$ will suffice for a worst case condition.

Output load current will be divided based on the output resistance of the individual buffers. Therefore, the available output current will not quite be doubled unless output resistances are matched. As for offset voltage, the 25°C limits should be used for worst case calculations.

Parallel operation is not thermally unstable. Should one unit get hotter than its mates, its share of the output and its standby dissipation will decrease.

As a practical matter, parallel connection needs only some increased attention to heat sinking. In some applications, a few ohms equalization resistance in each output may be wise. Only the most demanding applications should require matching, and then just of output resistance at 25°C.

Isolating Capacitive Loads



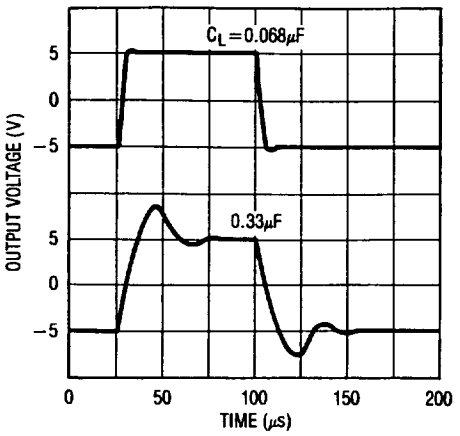
The inverting amplifier above shows the recommended method of isolating capacitve loads. Non-inverting amplifiers are handled similarly.

At lower frequencies, the buffer is within the feedback loop so that its offset voltage and gain errors are negligible. At higher frequencies, feedback is through C_f, so that phase shift from the load capacitance acting against the buffer output resistance does not cause loop instability.

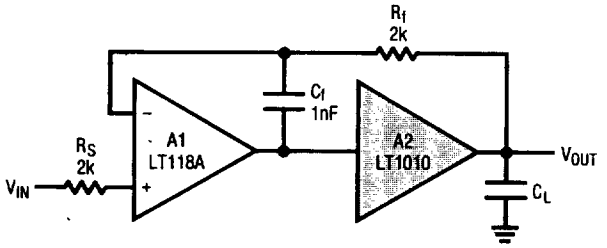
Stability depends upon the R_fC_f time constant, or the closed loop bandwidth. With an 80kHz bandwidth, ringing is negligible for $C_L = 0.068\mu F$ and damps rapidly for $C_L = 0.33\mu F$. The pulse response is shown in the graph.

APPLICATIONS INFORMATION

Pulse Response



Small signal bandwidth is reduced by C_f, but considerable isolation can be obtained without reducing it below the power bandwidth. Often, a bandwidth reduction is desirable to filter high frequency noise or unwanted signals.

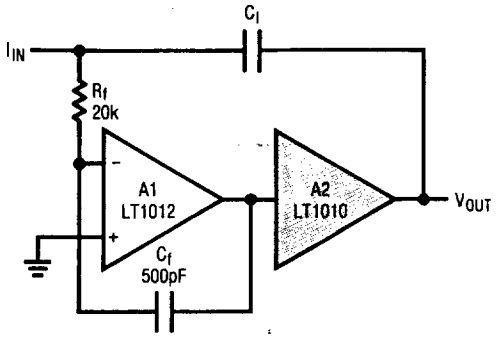


The follower configuration is unique in that capacitive load isolation is obtained without a reduction in small signal bandwidth, although the output impedance of the buffer comes into play at high frequencies. The precision unity-gain buffer above has a 10MHz bandwidth without capacitive loading, yet it is stable for all load capacitance to over 0.3μF, again determined by R_fC_f.

This is a good example of how fast op amps can be made quite easy to use by employing an output buffer.

Integrator

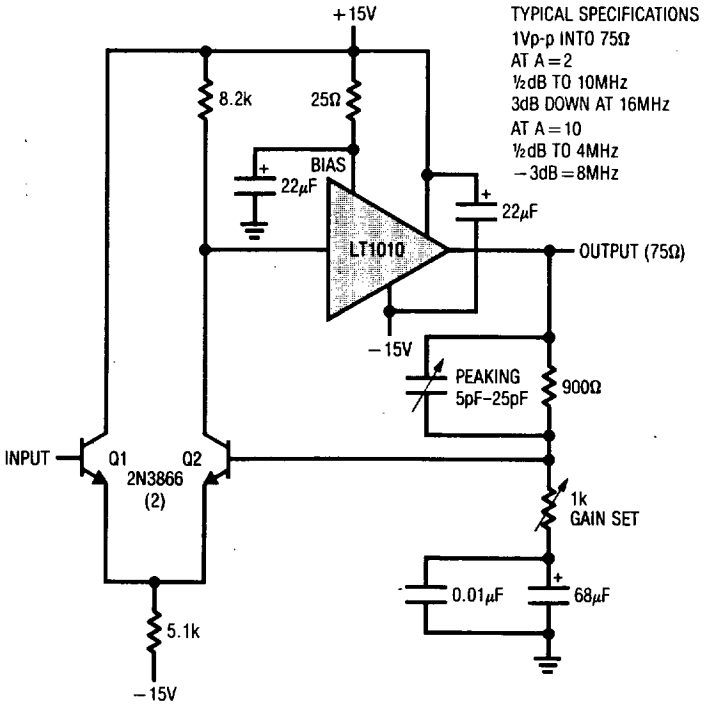
A low pass amplifier can be formed just by using large C_f in the inverter described earlier, as long as the increasing closed loop output impedance above the cutoff frequency is not a problem and the op amp is capable of supplying the required current at the summing junction.



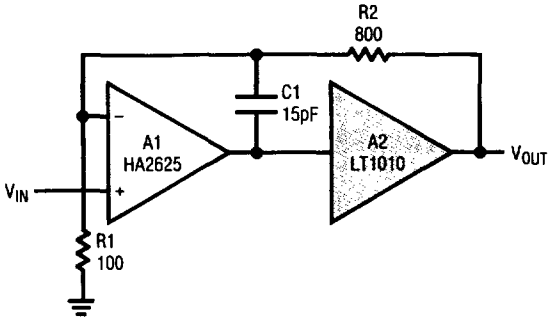
If the integrating capacitor must be driven from the buffer output, the circuit above can be used to provide capacitive load isolation. As before, the stability with large capacitive loads is determined by R_fC_f.

Wideband Amplifiers

This simple circuit provides an adjustable gain video amplifier which will drive 1Vp-p into 75Ω. The differential pair provides gain, with the LT1010 serving as an output stage. Feedback is arranged in the conventional manner, although the 68μF – 0.01 combination limits dc gain to unity for all gain settings. For applications sensitive to NTSC requirements, dropping the 25Ω output stage bias value will aid performance.



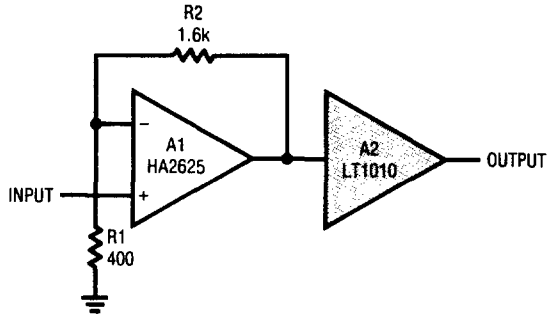
APPLICATIONS INFORMATION



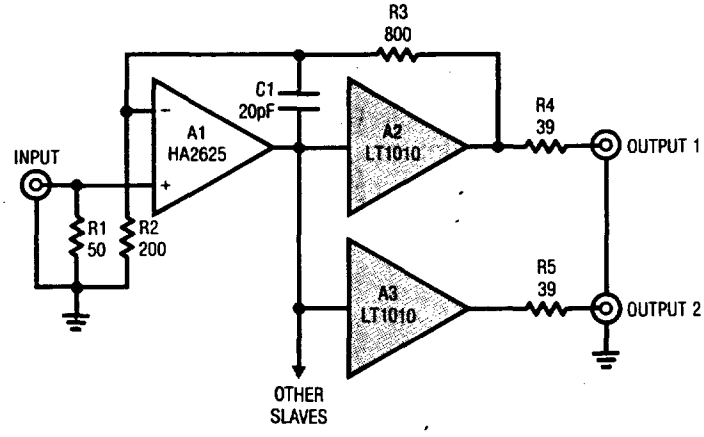
This shows the buffer being used with a wideband amplifier that is not unity-gain stable. In this case, C1 cannot be used to isolate large capacitive loads. Instead, it has an optimum value for a limited range of load capacitances.

The buffer can cause stability problems in circuits like this. With the TO-3 and TO-220 packages, behavior can be improved by raising the quiescent current with a 20Ω resistor from the bias terminal to V^+. Alternately, devices in the TO-39 package or miniDIP can be operated in parallel.

It is possible to improve capacitive load stability by operating the buffer class-A at high frequencies. This is done by using quiescent current boost and bypassing the bias terminal to V^- with more than 0.02μF.



Putting the buffer outside the feedback loop as shown here will give capacitive load isolation, with large output capacitors only reducing bandwidth. Buffer offset, referred to the op amp input, is divided by the gain. If the load resistance is known, gain error is determined by the output resistance tolerance. Distortion is low.



The 50Ω video line splitter here puts feedback on one buffer, with the others slaved. Offset and gain accuracy of slaves depend on their matching with master.

When driving long cables, including a resistor in series with the output should be considered. Although it reduces gain, it does isolate the feedback amplifier from the effects of unterminated lines which present a resonant load.

When working with wideband amplifiers,special attention should *always* be paid to supply bypassing, stray capacitance and keeping leads short. Direct grounding of test probes, rather than the usual ground lead, is absolutely necessary for reasonable results.

The LT1010 has slew limitations that are not obvious from standard specifications. Negative slew is subject to glitching, but this can be minimized with quiescent current boost. The appearance is always worse with fast rise signal generators than in practical applications.

APPLICATIONS INFORMATION

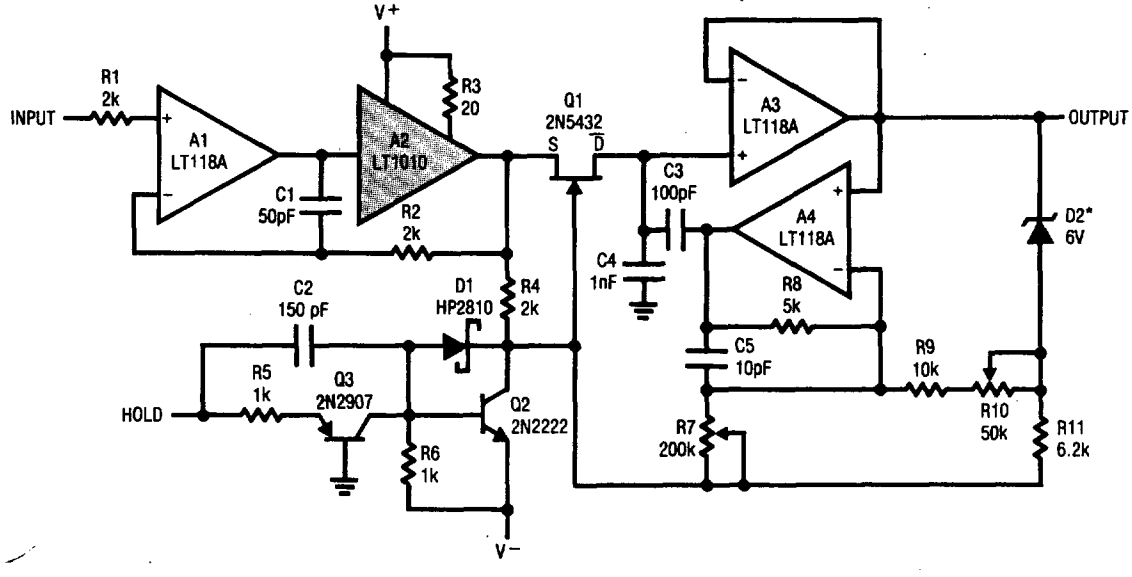
Track and Hold

The 5MHz track and hold shown here has a 400kHz power bandwidth driving ±10V. A buffered input follower drives the hold capacitor, C4, through Q1, a low resistance FET switch. The positive hold command is supplied by TTL logic, with Q3 level shifting to the switch driver, Q2. The output is buffered by A3.

When the gate is driven to V⁻ for HOLD, it pulls charge out of the hold capacitor. A compensating charge is put into the hold capacitor through C3. The step into hold is made independent of the input level with R7 and adjusted to zero with R10.

Since internal dissipation can be quite high when driving fast signals into a capacitive load, using a buffer in a power package is recommended. Raising buffer quiescent current to 40mA with R3 improves frequency response.

This circuit is equally useful as a fast acquisition sample and hold. An LF156 might be used for A3 to reduce drift in hold because its lower slew rate is not usually a problem in this application.

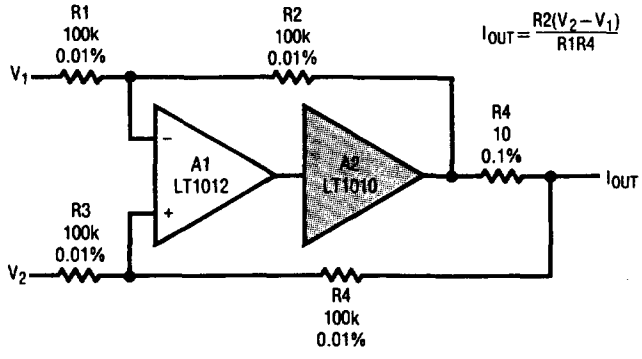


*2N2369 EMITTER BASE JUNCTION

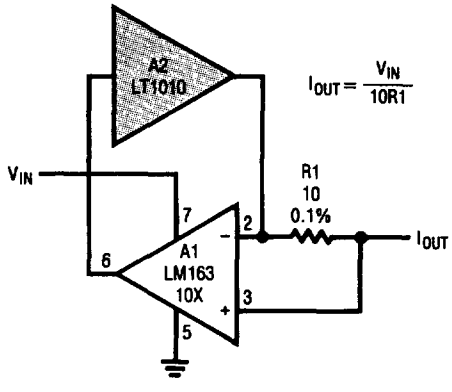
APPLICATIONS INFORMATION

Current Sources

A standard op amp voltage to current converter with a buffer to increase output current is shown here. As usual, excellent matching of the feedback resistors is required to get high output resistance. Output is bi-directional.



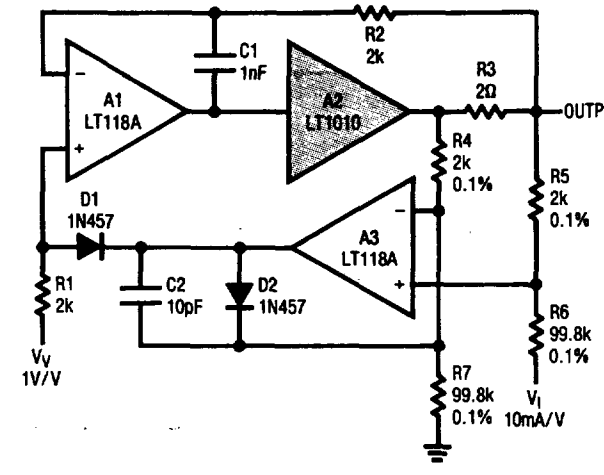
This circuit uses an instrumentation amplifier to eliminate the matched resistors. The input is not high impedance and must be driven from a low impedance source like an op amp. Reversal of output sense can be obtained by grounding pin 7 of the LM163 and driving pin 5.



Output resistances of several megohms can be obtained with both circuits. This is impressive considering the ±150mA output capability. High frequency output characteristics will depend on the bandwidth and slew rate of the amplifiers. Both these circuits have an equivalent output capacitance of about 30nF.

Voltage/Current Regulator

This circuit regulates the output voltage at V_V until the load current reaches a value programmed by V_I. For heavier loads, it is a precision current regulator.



With output currents below the current limit, the current regulator is disconnected from the loop by D1, with D2 keeping its output out of saturation. This output clamp enables the current regulator to get control of the output current from the buffer current limit within a microsecond for an instantaneous short.

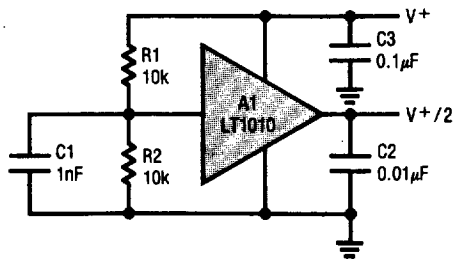
In the voltage regulation mode, A1 and A2 act as a fast voltage follower using the capacitive load isolation technique described earlier. Load transient recovery as well as capacitive load stability are determined by C1. Recovery from short circuit is clean.

Bi-directional current limit can be obtained by adding another op amp connected as a complement to A3.

APPLICATIONS INFORMATION

Supply Splitter

Dual supply op amps and comparators can be operated from a single supply by creating an artificial ground at half the supply voltage. The supply splitter shown here can source or sink 150mA.

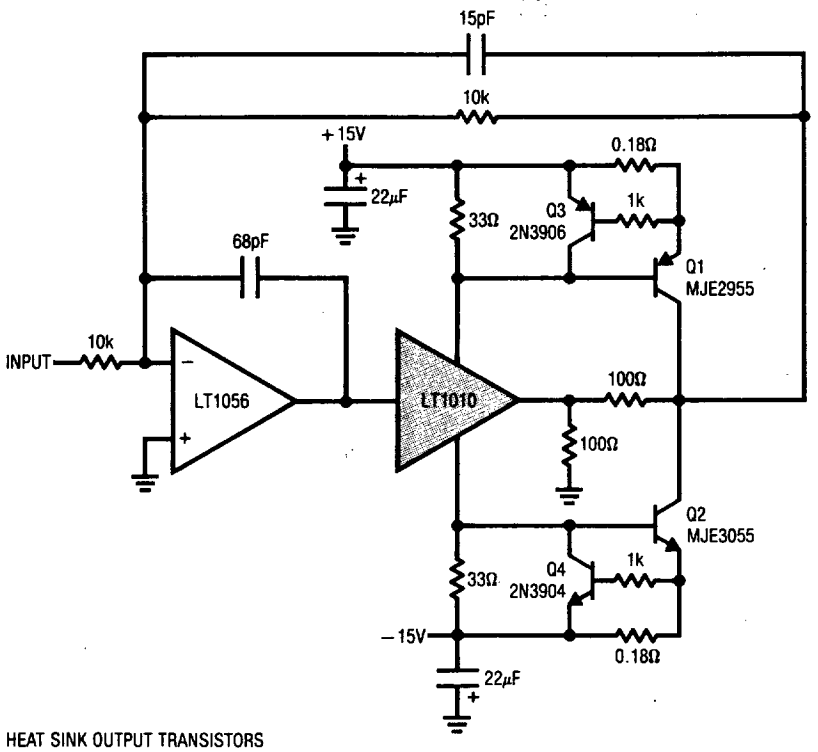


The output capacitor, C2, can be made as large as necessary to absorb current transients. An input capacitor is also used on the buffer to avoid high frequency instability that can be caused by high source impedance.

High Current Booster

The circuit below uses a discrete stage to get 3A output capacity. The configuration shown provides a clean, quick way to increase LT1010 output power. It is useful for high current loads, such as linear actuator coils in disk drives.

The 33Ω resistors sense the LT1010's supply current, with the grounded 100Ω resistor supplying a load for the LT1010. The voltage drop across the 33Ω resistors biases Q1 and Q2. Another 100Ω value closes a local feedback loop, stabilizing the output stage. Feedback to the LT1056 control amplifier is via the 10k value. Q3 and Q4, sensing across the 0.18Ω units, furnish current limiting at about 3.3A.



HEAT SINK OUTPUT TRANSISTORS

Wideband FET Input Stabilized Buffer

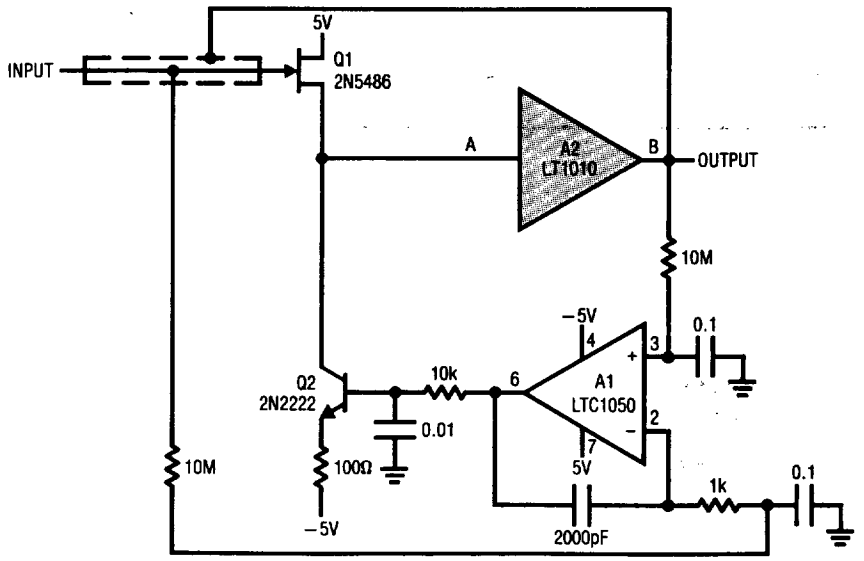
The figure below shows a highly stable unity gain buffer with good speed and high input impedance. Q1 and Q2 constitute a simple, high speed FET input buffer. Q1 functions as a source follower, with the Q2 current source load setting the drain-source channel current. The LT1010 buffer provides output drive capability for cables or whatever load is required. Normally, this open loop configuration would be quite drifty because there is no dc feedback. The LTC1050 contributes this function to stabilize the circuit. It does this by comparing the filtered circuit output to a similarly filtered version of the input signal. The amplified difference between these signals is used to set Q2's bias, and hence Q1's channel current. This forces Q1's V_{GS} to whatever voltage is required to match the circuit's input and output potentials. The 2000pF capacitor at A1 provides stable loop compensation. The RC network in A1's output prevents it from seeing high speed edges coupled through Q2's collector-base junction. A2's output is also fed back to the shield around Q1's gate lead, bootstrapping the circuit's effective input capacitance down to less than 1pF.

Gain Trimmable Wideband FET Amplifier

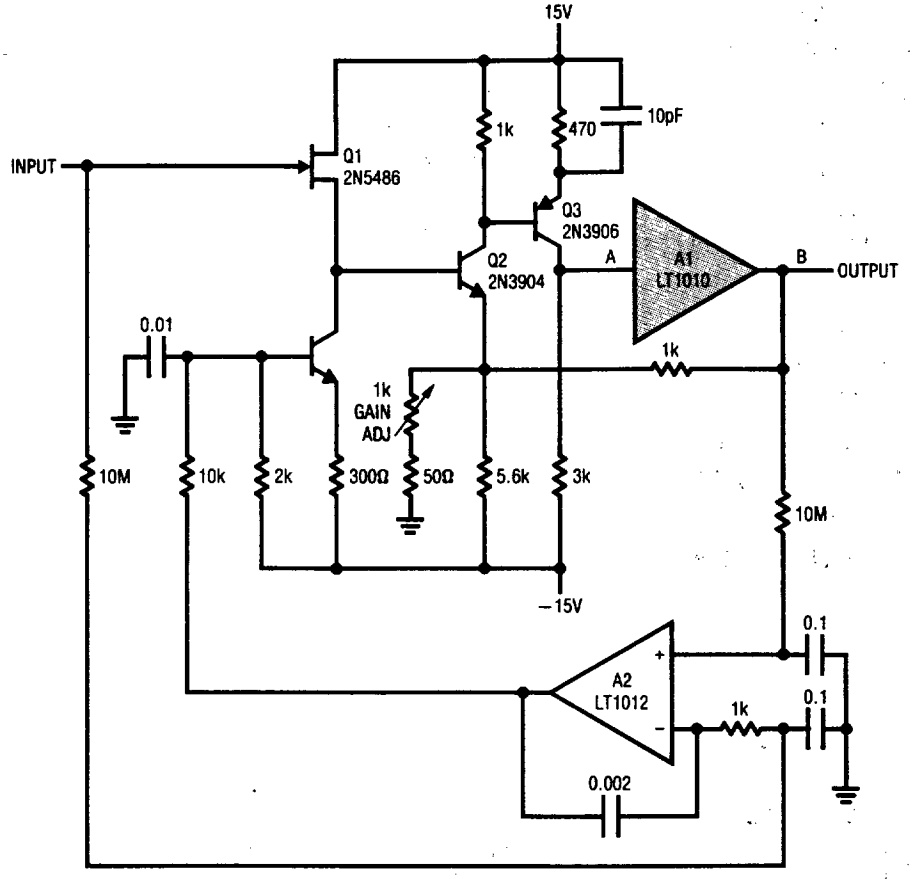
A potential difficulty with the previous circuit is that the gain is not quite unity. The figure labelled (A) on the next page maintains high speed and low bias while achieving a true unity gain transfer function.

This circuit is somewhat similar, except that the Q2-Q3 stage takes gain. A2 dc stabilizes the input-output path, and A1 provides drive capability. Feedback is to Q2's emitter from A1's output. The 1k adjustment allows the gain to be precisely set to unity. With the LT1010 output stage slew and full power bandwidth (1Vp-p) are 100V/μs and 10MHz, respectively. –3dB bandwidth exceeds 35MHz. At A = 10 (e.g., 1k adjustment set at 50Ω) full power bandwidth stays at 10MHz while the –3dB point falls to 22MHz.

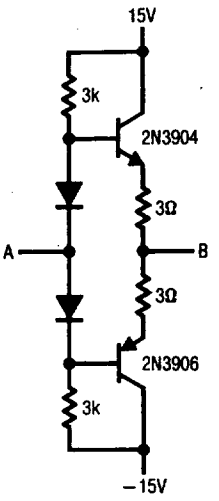
With the optional discrete stage, slew exceeds 1000V/μs and full power bandwidth (1Vp-p) is 18MHz. –3dB bandwidth is 58MHz. At A = 10, full power is available to 10MHz, with the –3dB point at 36MHz.



Figures A and B show response with both output stages. The LT1010 is used in Figure A (Trace A = input, Trace B = output). Figure B uses the discrete stage and is slightly faster. Either stage provides more than adequate performance for driving video cable or data converters, and the LT1012 maintains dc stability under all conditions.



(A)



(B)

Gain Trimmable Wideband FET Amplifier

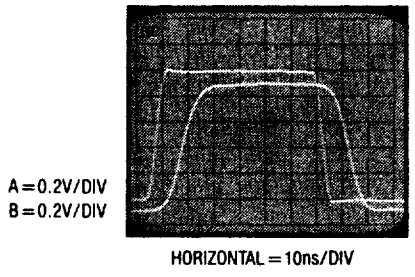


Figure A. Waveforms Using LT1010

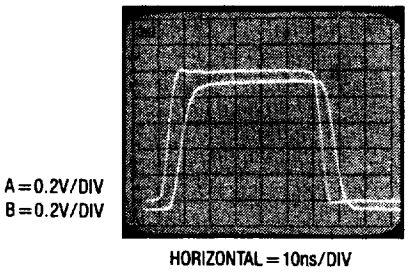


Figure B. Waveforms Using Discrete Stage

DEFINITION OF TERMS

Output Offset Voltage: The output voltage measured with reference to the input.

Input Bias Current: The current out of the input terminal.

Large Signal Voltage Gain: The ratio of the output voltage change to the input voltage change over the specified input voltage range.

Output Resistance: The ratio of the change in output voltage to the change in load current producing it.*

Output Saturation Voltage: The voltage between the output and the supply rail at the limit of the output swing toward that rail.

Saturation Offset Voltage: The output saturation voltage with no load.

Saturation Resistance: The ratio of the change in output saturation voltage to the change in current producing it, going from no load to full load.*

Slew Rate: The average time rate of change of output voltage over the specified output range with an input step between the specified limits.

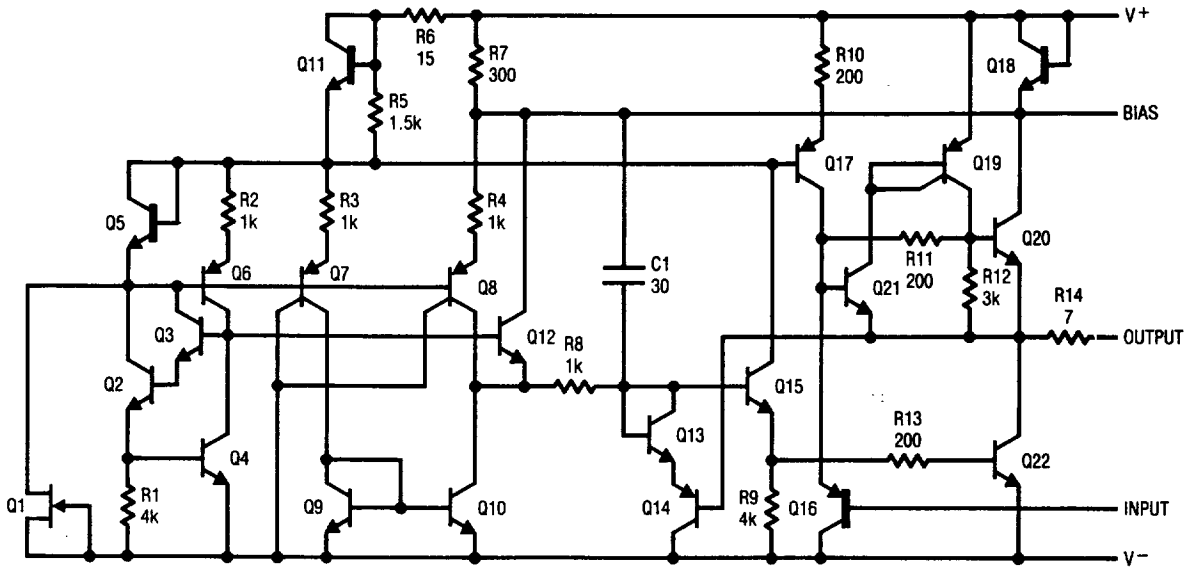
Bias Terminal Voltage: The voltage between the bias terminal and V^+.

Supply Current: The current at either supply terminal with no output loading.

*Pulse measurements (~1ms) as required to minimize thermal effects.

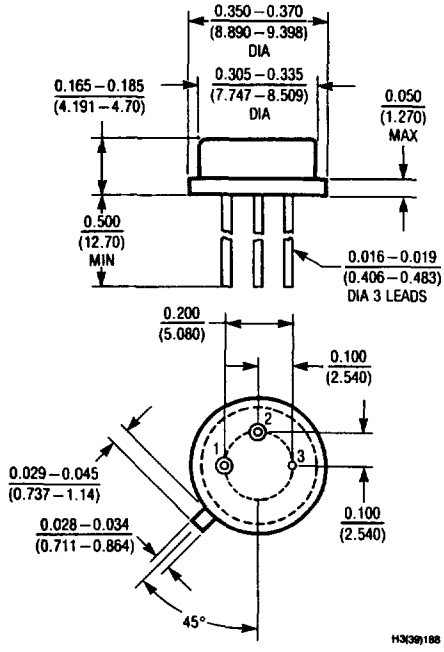
2

SCHEMATIC DIAGRAM (excluding protection circuits)



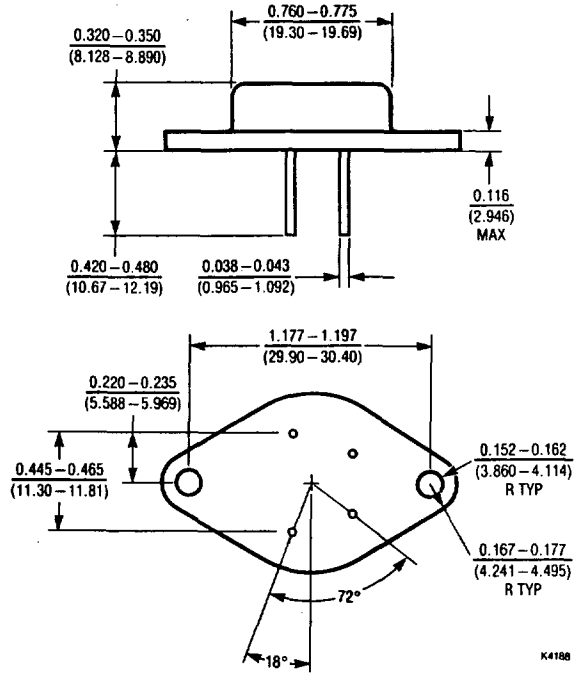
PACKAGE DESCRIPTION Dimensions in inches (millimeters) unless otherwise noted.

H Package
4-Lead TO-39 Metal Can
(Kovar Base)



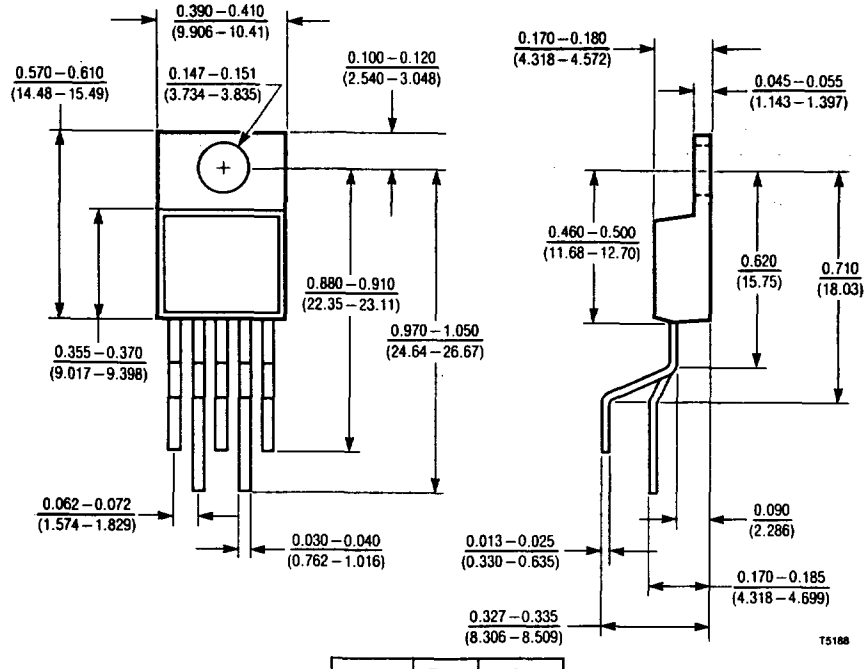
	T_{jmax}	θ_{jc}
LT1010M	150°C	40°C/W
LT1010C	125°C	40°C/W

K Package
4-Lead TO-3 Metal Can
(Steel)



	T_{jmax}	θ_{jc}
LT1010M	150°C	25°C/W
LT1010C	125°C	25°C/W

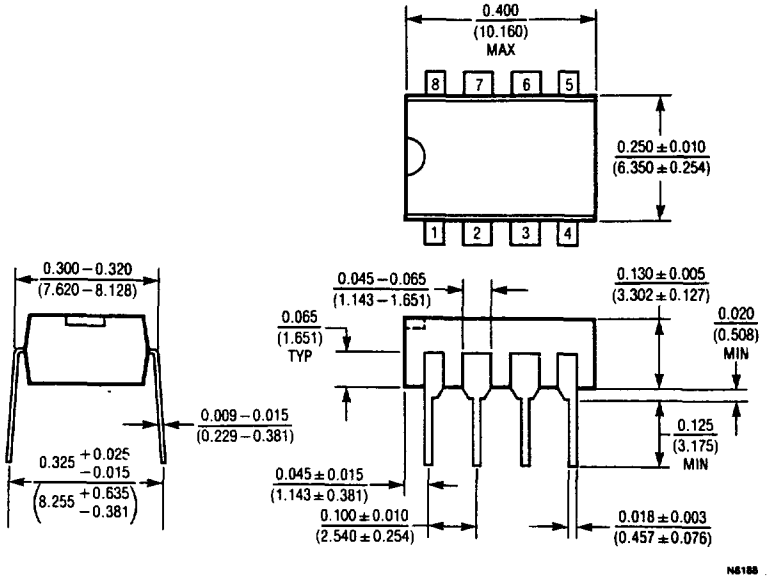
T Package
5-Lead TO-220 Plastic



	T_{jmax}	θ_{jc}
LT1010C	125°C	25°C/W

PACKAGE DESCRIPTION Dimensions in inches (millimeters) unless otherwise noted.

N Package
8-Lead Plastic DIP



T_{jmax}	θ_{jc}
150°C	130°C/W